Laboratory #5
Current and Voltage Source

I. Objectives

1. Review the MOSFET characteristics and transfer function.
2. Understand the relationship between the bias, the input signal and the output response.
3. Understand the MOSFET biasing techniques.
4. Understand current and voltage source.

II. Components and Instruments

1. Components
   (1) MOSFET array IC : CD4007 ×1
   (2) OPAMP IC : LM324 ×1
   (3) Resistor : 100Ω ×1, 1kΩ ×1, 2kΩ ×1, 4.7kΩ ×4, 5.1kΩ ×2, 10kΩ ×2, 20kΩ ×2, 47 kΩ×1, 100kΩ ×1
2. Instruments
   (1) DC power supply (Keysight E36311A)
   (2) Digital multimeter (Keysight 34450A)

III. Reading

1. Section 5.1-5.7 of the Textbook “Microelectronic Circuits, 6th edition, Sedra/Smith”.

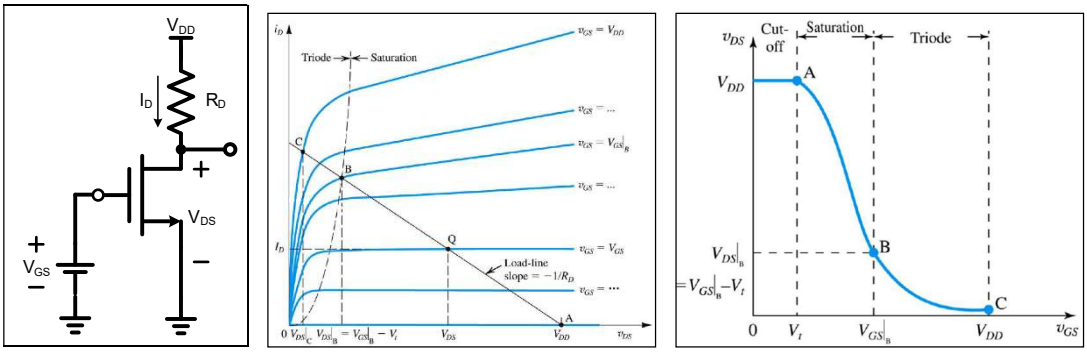
IV. Preparation

Nowadays, there are more and more complicated functions can be implemented using MOSFETs in VLSI circuits. But no matter how complicated the functions are, all of them are realized by combining the processes of addition, subtraction, and amplification on the voltage and current signals. In practical circuits design, at first, the operating points (bias points) for MOSFETs should be decided so that all functional blocks can operate correctly within the required dynamic range. As the result, the MOSFET biasing is an important issue for circuit design. In the following sections, the concept of MOSFET biasing and some basic MOSFET biasing methods will be introduced.

1. The MOSFET Transfer Characteristics

Taking CS amplifier as an example (as shown in Fig. 5.1(a)), the transfer function of

v_{DS} vs. v_{GS} can be derived from Fig. 5.1(b). If there is no voltage applied to the gate (v_{GS}=0), then no current will flow through R_D and v_{DS} is equal to v_{DD}. When v_{GS} exceeds the threshold voltage V_t, the current begins to increase and v_{DS} becomes lower because of the higher voltage drop on R_D. Based on the relationship between v_{GS}, v_{DS} and i_D in saturation region, the operating point will move from point A to point B. The MOSFET continues operating in saturation region until v_{GS}>v_{DS}+V_t. After point B, the output voltage decrease slowly toward zero. Here we identify a particular operating point C as V_{GS}=V_{DD}. The corresponding output voltage V_{OC} will usually be very small. This point-by-point determination of the transfer characteristics results in the transfer curve shown in Fig. 5.1 (c).



(a) (b) (c)

Fig. 5.1 (a) NMOS with a load resistor R_D (b) i_D vs. v_{DS} under different v_{GS} (c) NMOS transfer function.

The MOSFET is biased in different regions for different applications. For example, if the MOSFET is used to provide the function of amplification, it should be biased in the saturation region because of its maximal slope (which means maximal gain). After the biasing voltage of V_{GS} has been set, small signal v_{gs} is applied to the input, the output response of v_{DS} can then be observed at the drain of MOSFET. As shown in Fig. 5.2, the input signal is the combination of V_{GS} and v_{gs}.

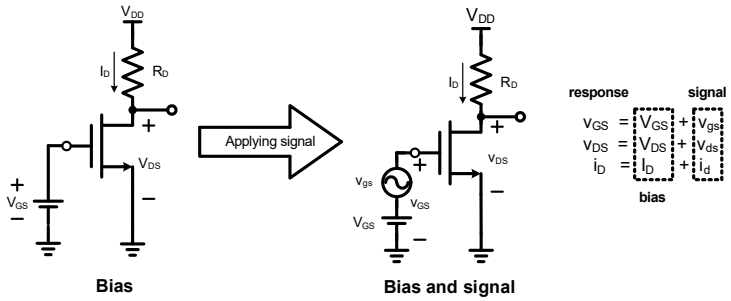


Fig. 5.2 Combination of bias and signal.

2. Biasing in MOSFET Amplifier Circuits

As mentioned in the previous section, the establishment of an appropriate DC operating point is an essential step in the design of a MOSFET amplifier circuit. This is the step known as biasing design. An appropriate DC operating point or bias point should ensure the operation in the saturation region for all expected input-signal levels, which is characterized by a stable and predictable DC drain current I_D, and by a DC drain-to-source voltage V_{DS} that.

(1) Biasing by fixed V_{GS}

The most straightforward approach to bias a MOSFET is to fix its gate-to-source voltage V_{GS} at the required value and so the desired I_D. This voltage value can simply be derived from the supply voltage V_{DD} through the use of an appropriate voltage divider. Alternatively, it can be derived from any another suitable reference voltage available in the system. However, this is not a good technique in biasing a MOSFET. Recall that,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 \quad \text{..... (Eq. 5.1)}$$

and note that the values of V_t, C_{ox} and W/L vary widely for the same devices, since the process variation. Furthermore, both V_t and μ_n is temperature-dependent, and the I_D is thus temperature-sensitive. To emphasize that MOSFET biasing by fixed V_{GS} is not a good technique, here in Fig. 5.3, we show the extreme case of i_D-v_{GS} characteristic curves of two same type MOSFETs in a batch. As the value of V_{GS} is fixed, it will correspond to different drain current due to the process variation.

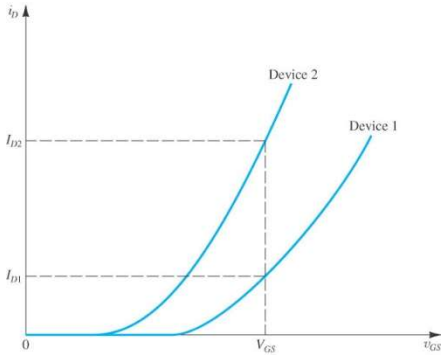


Fig. 5.3 The use of fixed bias (constant V_{GS}) can result in a large variation in the value of I_D.

(2) Biasing by fixing V_G with source degeneration

A better biasing technique for discrete MOSFET circuits is to connect a resistor with the source lead while fixing the gate voltage V_G, as shown in Fig. 5.4 (a). For this circuit we can write

$$V_G = V_{GS} + R_S I_D \quad \text{..... (Eq. 5.2)}$$

If V_G is much greater than V_{GS}, I_D will then be determined by the values of V_G and R_S. However, even if V_G is not much larger than V_{GS}, the resistor R_S provides negative feedback and stabilize the value of the bias current I_D. This could be understood that since V_G is constant, V_{GS} will decrease as I_D increases, and this in turn results in a decrease in I_D. This negative feedback function of R_S gives it the name **degeneration resistor**. Fig. 5.4 (b) provides a graphical illustration of the effectiveness of this biasing scheme, where the intersection of the straight line of (Eq. 5.2) and the i_D-v_{GS} characteristic curve provides the coordinates of the bias point. Compared to the case of fixed V_{GS}, the variation in I_D is much smaller. Also, note that the variation decreases as V_G and R_S are made larger, since this results in flatter slope.

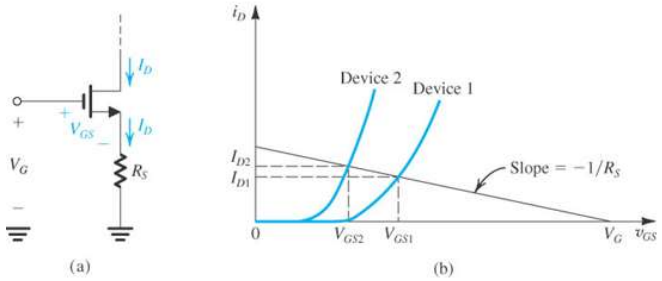


Fig. 5.4 Biasing using a fixed voltage with degeneration resistance
(a) basic arrangement; (b) reduced variability in I_D

(3) Biasing with drain-to-gate feedback resistor

Another simple MOSFET biasing circuit is to utilize a feedback resistor to connect between the drain and the gate as shown in Fig. 5.5. Here the large feedback resistance R_G (usually in range of MΩ) forces the DC voltage at the gate to be equal to that at the drain (because I_G=0). For this circuit, it can be expressed as follows.

$$V_{DD} = V_{GS} + I_D R_D \quad \text{..... (Eq. 5.3)}$$

which is similar to Eq. 5.2, and it has the same mechanism as the biasing scheme discussed in Fig. 5.4 (a). If I_D changes for some reason, say increases, V_{GS} will decrease according to Eq. 5.3. Thus the negative feedback function or degeneration provided by R_G works to keep the value of I_D as constant as possible.

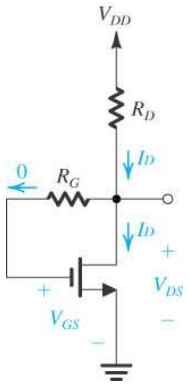


Fig. 5.5 Biasing MOSFET using feedback resistance, R_G

The biasing circuit of Fig. 5.5 can directly be utilized in CS amplifier. Apply the input voltage signal to the gate via a coupling capacitor for not disturbing the DC bias conditions, and the amplified output signal at the drain can also be coupled to another part of the circuit via another capacitor.

(4) Biasing using current mirror

The most effective scheme for biasing a MOSFET amplifier is the using of a constant-current source, which is as shown in Fig. 5.6 (a). Resistor R_D establishes an appropriate DC voltage at the drain to allow for the required output signal swing while ensuring that the transistor always remains in the saturation region.

A circuit for implementing the constant-current source I is shown in Fig. 5.6 (b). The key-point of the circuit is the transistor Q_1, whose drain is shorted to its gate and is thus operated in the saturation region, such that

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2 \quad \text{..... (Eq. 5.4)}$$

In Eq. 5.4, we have neglected channel-length modulation. The drain current of Q_1 is supplied by V_{DD} through resistor R. Since the gate current is zero, the drain current of Q_1 will be

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R} \quad \text{..... (Eq. 5.5)}$$

where the current through R could be considered as the reference current of the current source and denoted as I_{REF}. Eq. 5.4 and Eq. 5.5 can be used to determine the value of R, once the parameter values of Q_1 and the desired value for I_{REF} are given. Now consider the transistor Q_2, which has the same V_{GS} as Q_1, its drain current can be expressed as Eq. 5.6 if Q_2 is ensured to be operated in saturation region.

$$I = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2 \quad \text{..... (Eq. 5.6)}$$

In Eq. 5.6, we have neglected channel-length modulation. Eq. 5.5 and Eq. 5.6 enables us to relate the current I to the reference current I_{REF},

$$I = I_{REF}\frac{(W/L)_2}{(W/L)_1} \quad \text{..... (Eq. 5.7)}$$

This circuit, which is known as a **current mirror**, is very popular in the design of IC MOSFET amplifiers.

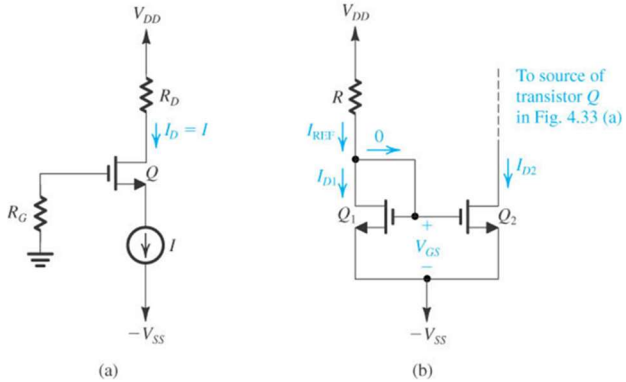


Fig. 5.6 (a) MOSFET biasing using a constant-current source I.
(b) Constant-current source I implemented by current mirror.

(5) Biasing using voltage-controlled current source

Since each MOSFETs and passive components has process deviation, the currents that a current mirror generates might not be accurate enough. Additionally, the noise on the power supply rails will cause variation on the generated current.

Due to the errors that is mentioned above, using a current mirror to generate a constant current is not robust enough. To design a better current source, we need to make output current of current source less independent of component. A circuit for implementing a voltage-controlled current source is shown in Fig. 5.7. A OPAMP in closed-loop is included. The key-points of the circuit is the OPAMP that connects its negative input terminal to the source of Q1. Consider the OPAMP is ideal (Bandwidth→∞, Gain→∞), the positive and negative terminals of the OPAMP are virtual-shorted, the load current I_{OUT} can be derived as

$$I_{OUT} = \frac{V_{in}}{R_D} \text{.....(Eq. 5.8)}$$

It can be seen that the value of load current I_{OUT} only depends on input voltage V_{in} and the resistor R_D, so it's a voltage-controlled current source. The advantage of the circuit in Fig. 5.7 is that the variation at output can be compensated by the negative feedback. For example, if the load resistor R_D is changed to a larger value, it will make drain voltage of Q_1 increases. Then, since the positive terminal of OPAMP, which is equal to drain voltage of Q_1, increases at the moment, the output of OPAMP will increases, resulting in the current flowing through the PMOS Q_1 decreases and equals I_{OUT} finally.

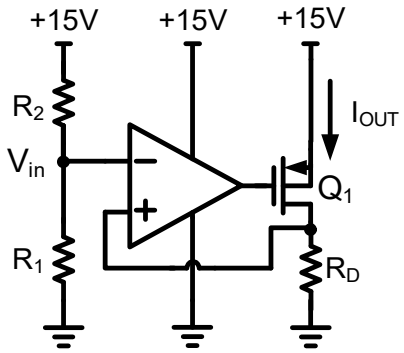


Fig. 5.7 Voltage-controlled current source

(6) Biasing using current-controlled voltage source

A simple single resistor can be used to convert a current into voltage. But the voltage will not be able to directly drive other stage. To generate a more stable voltage source, a buffer amplifier or a reference current is usually needed. A circuit for implementing a current-controlled voltage source is shown in Fig. 5.8. It produces an output voltage V_{OUT} from input current I_{IN}. The output voltage V_{OUT} can be derived as

$$V_{out}=I_{in}R_L \text{.....(Eq. 5.9)}$$

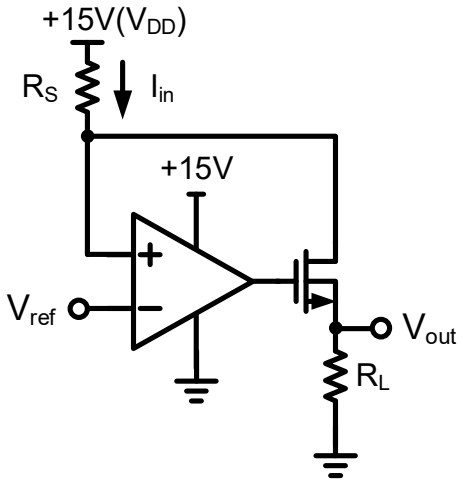


Fig. 5.8 Current-controlled voltage source

V. Explorations

The layout and connections of CD4007 MOS array are shown in Fig. 5.9. CD4007 consists of 6 transistors, 3 are p-channel and another 3 are n-channel, which are connected in some nodes in order to reduce the number of IC pins required, but otherwise fairly flexible.

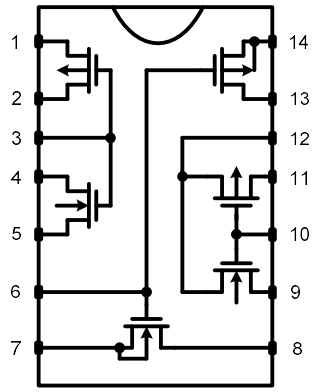


Fig. 5.9 Pin diagram of CD4007

NOTE: Pin14 must be connected to the most positive voltage, and pin 7 to the most negative. For the sake of safety, maintain the voltage between pin 7 and pin 14 at or below 16V to avoid internal voltage breakdown. **Make sure you turn off the power supply before changing any circuit connection**.

DVM: Digital Voltage Meter

DCM: Digital Current Meter

DMM: Digital Multi-Meter

1. PMOS Current Mirror

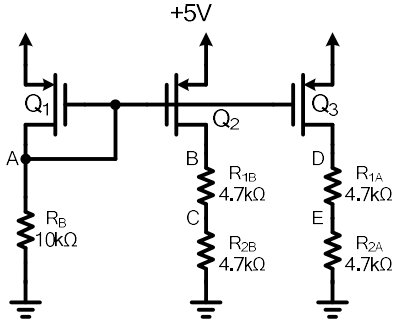


Fig. 5.10 A PMOS current mirror

(1) Assemble the PMOS current mirror as shown in Fig. 5.10.

(2) Use the DVM to measure the voltages at nodes A, B, C, D, E. Measure the **current transfer ratios** from input (A) to outputs (B and D) and record them in Table 5.1.

(3) Short R_{1A}, noting the old and new values, and particularly the change in voltage.

(4) Remove R_{1A} and R_{2A}, and short nodes B and D. Record the current flow through

point A and point B in Table 5.1 respectively.

2. Voltage-controlled current source

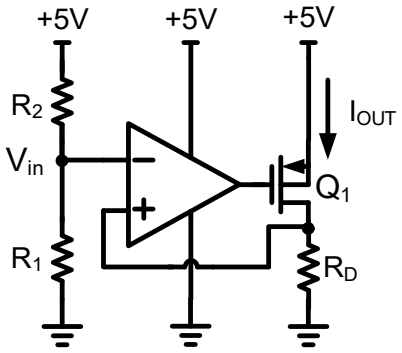


Fig. 5.11 Voltage-controlled current source

(1) Assemble the voltage-controlled current source as shown in above. (R_2=5.1 kΩ, 10kΩ, 20kΩ, 47kΩ, 100kΩ, R_1=20kΩ, R_D=10kΩ)

(2) Use the DVM to measure the voltages at nodes V_{in} and use DCM to measure the current I_{OUT}. Record them in Table 5.2.

(3) Change the resistor R_2 and repeat (2)

3. Current-controlled voltage source

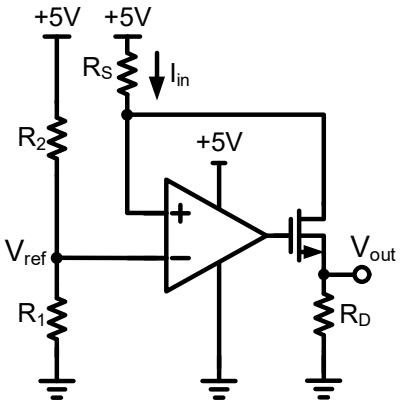


Fig. 5.12 Current-controlled voltage source

(1) Assemble the voltage-controlled current source as shown in above. (R_1=10kΩ, R_2=5.1kΩ, R_S=1kΩ, 2kΩ, 5.1kΩ, 10kΩ, 20k, R_D=100Ω)

(2) Use the DCM to measure the current I_{in} and use DVM to measure the current V_{out}. Record them in Table 5.3.

(3) Change the resistor R_S and repeat (2)

Laboratory #5 Pre-lab

Class:

Name: Student ID:

1. Problem 1 (PSPICE simulation)

Assemble the circuit as shown in Fig. 5.13. Use the bias point analysis to measure the voltage and current values at nodes A, B, C, D, and E.

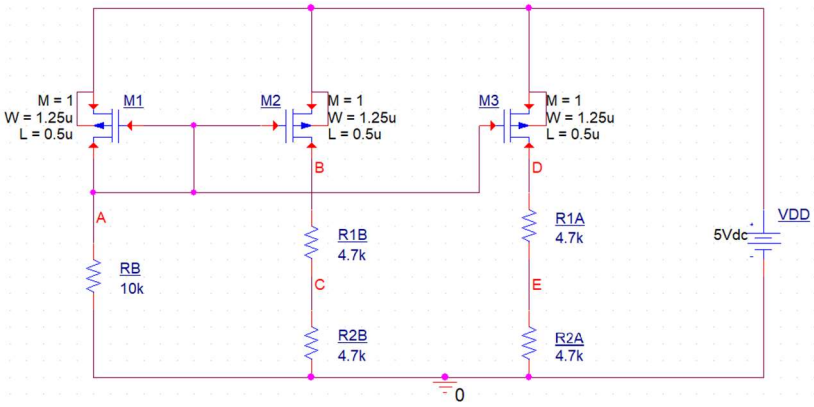


Fig. 5.13 PMOS-based current mirror

2. Problem 2 (PSPICE simulation)

Assemble the circuit as shown in Fig. 5.14. Use the bias point analysis to measure the voltage and current values V_{in} and I_{OUT}.

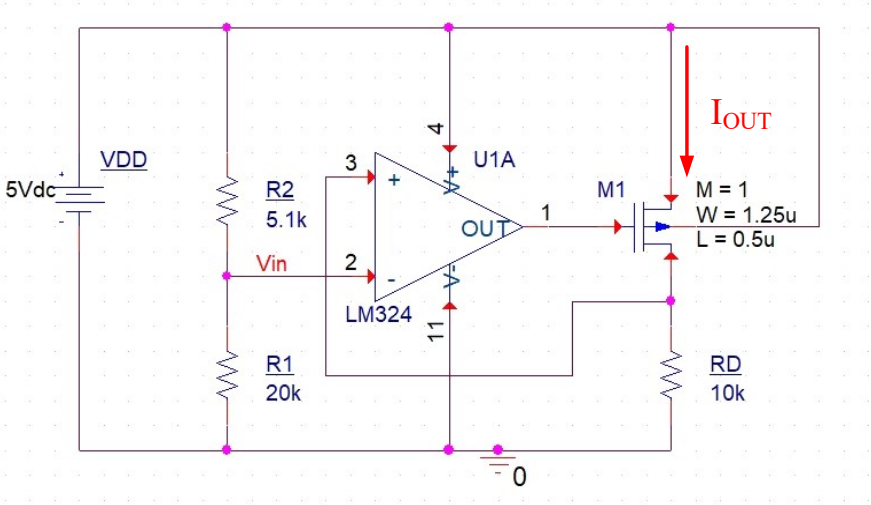


Fig. 5.14 Voltage-controlled current source

3. Problem 3 (PSPICE simulation)

Assemble the circuit as shown in Fig. 5.15. Use the bias point analysis to measure the current and voltage values I_{in} and V_{out}.

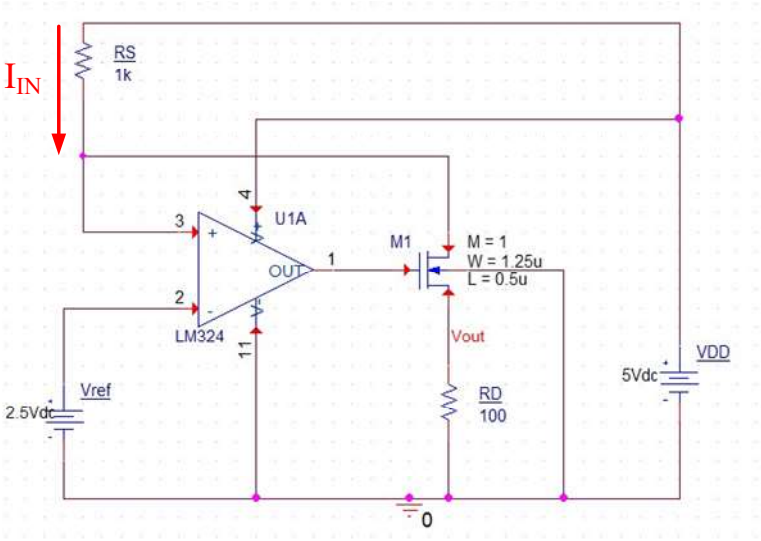


Fig. 5.15 Current-controlled current source

Laboratory #5 Report

Class:

Name: Student ID:

1. Exploration 1

Table 5.1

Bias point measurement					
Node	A	B	C	D	E
Voltage					
Current transfer ratio					
$\frac{I_B}{I_A}$			$\frac{I_D}{I_A}$		
Current transfer ratio (with R_{1A} shorting)					
$\frac{I_B}{I_A}$			$\frac{I_D}{I_A}$		
Current mirror (remove R_{XA} and connecting B and D)					
I_A			I_B		

2. Exploration 2

Table 5.2

R_2 (kΩ)	5.1	10	20	47	100
V_{in} (V)					
I_{OUT} (mA)					

3. Exploration 3

Table 5.3

R_S (kΩ)	1	2	5.1	10	20
I_{in} (mA)					
V_{out}(V)					

4. Problem 1

In Exploration 1, after removing R_{1A} and R_{2A}, does the current I_B become two times of I_A? If not, try to figure out the reasons.

5. Problem 2

Please try to explain the mechanism of the circuit Fig. 5.7 and list the advantages of the circuit over the Fig. 5.6.

6. Conclusion